

**Faculty of Engineering & Technology – Electrical & Computer Engineering Department**

**First Semester 2022 – 2023**

**Circuits and electronics lab**

**ENEE2103**

**PRELAB EXP.8**

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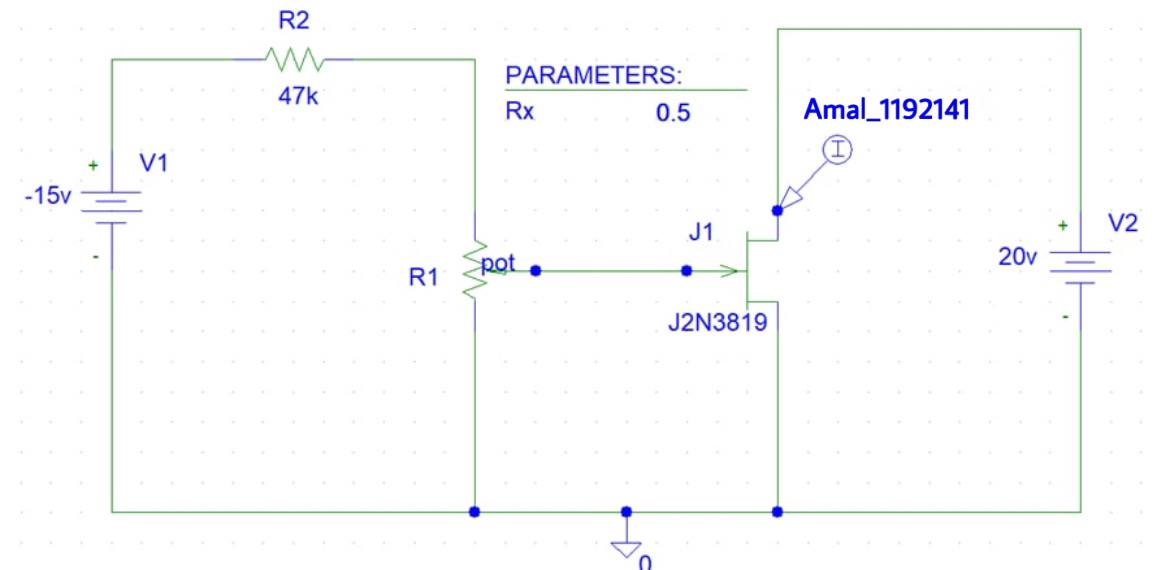
**Section: 2**

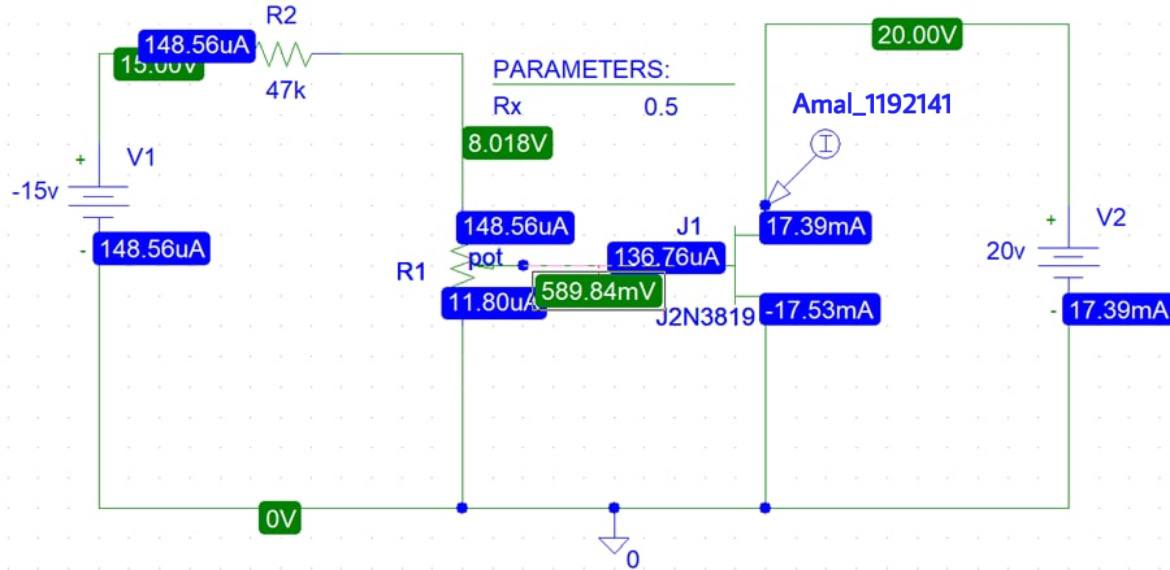
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**TA: Eng. Yazan Yousef**

**Date: 9th Dec 2022**

**Part A**: CHARACTERESTICS OF AN N-CHANNEL JFET





Simulation of ID





* Questions
* From your graph, above which values of VDS is ID almost unaffected by VDS when VGS=0?



(Vds,Ids)= (4.5691,16.811m)

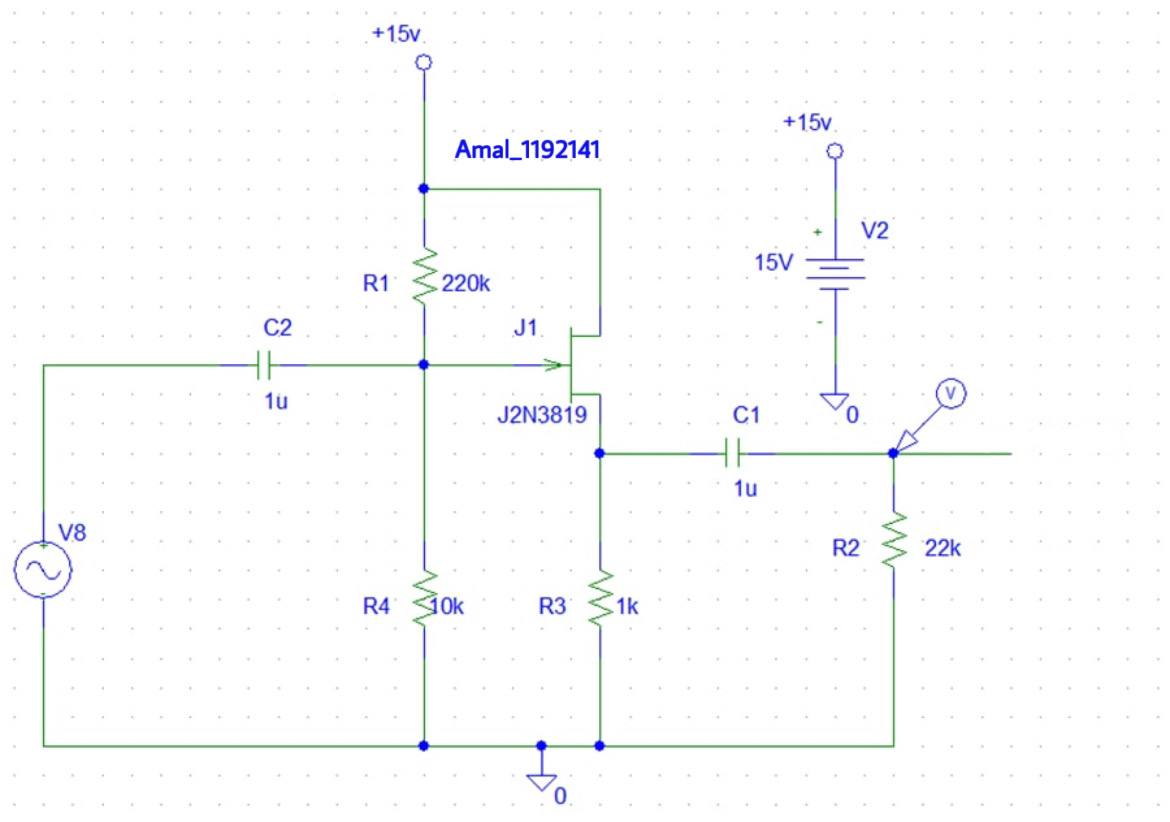
* For a given value of VDS , (say 10 V ),do equal changes of VGS cause equal changes of ID?

For a given value of Vds ,changes of Vgs doesn’t equal changes to Id

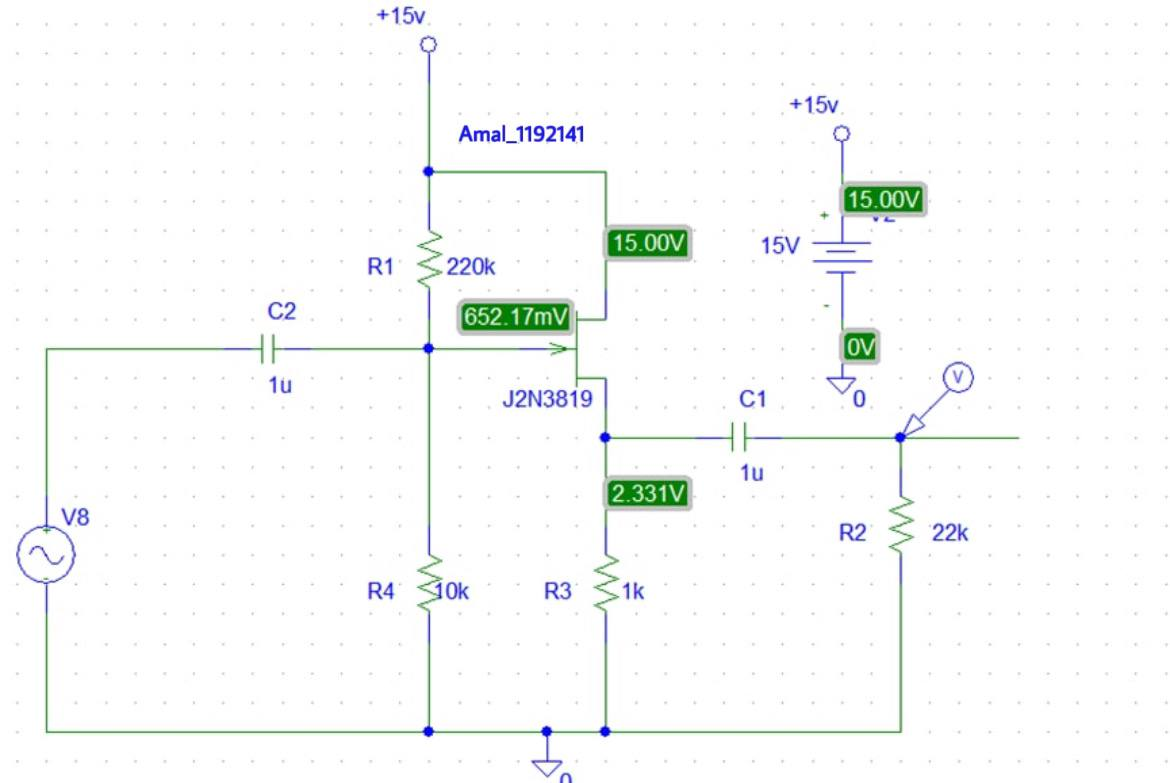
* Can you measure IG or is it too small?

It’s too small, so it’s very hard to measure it

**Part B :** COMMON DRAIN AMPLIFIER



- Bias point analysis



Vg= 652.17 mV

Vs=2.331 V

* Simulation of Vout



Av= 0.151/0.2=0.755

-Simulation of phase shift



In phase , phase difference =0 d

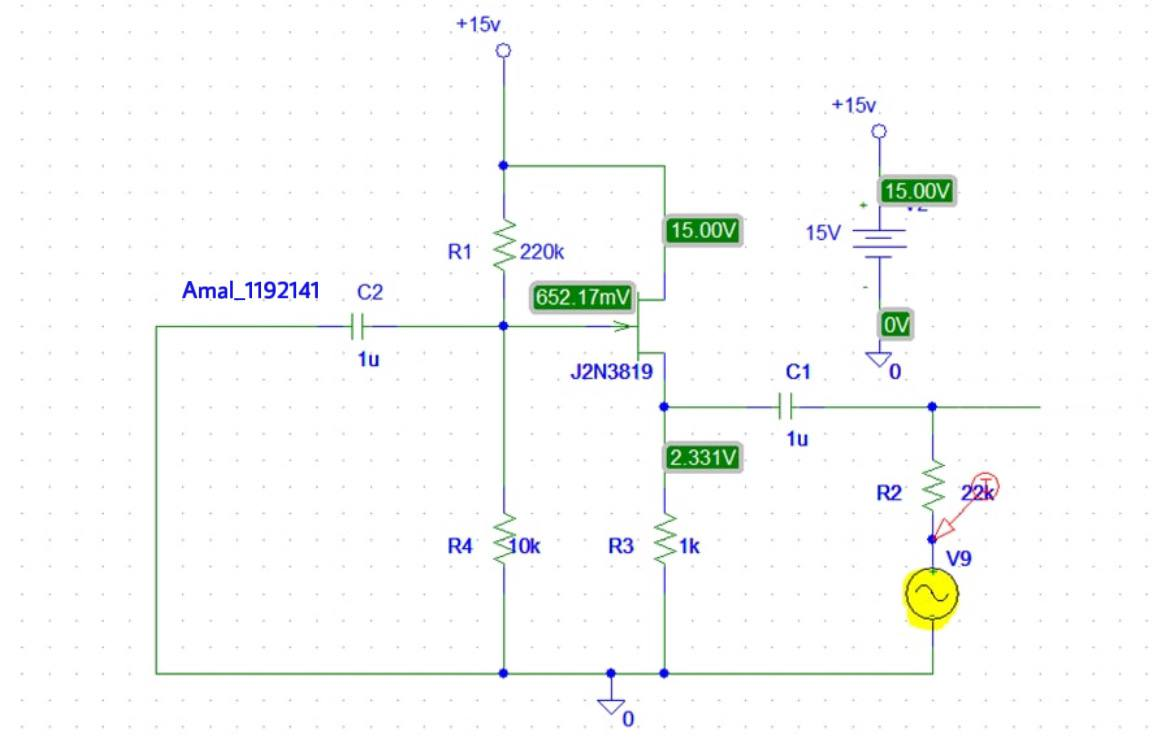
- Calculate Zin

- Simulation of Iin



Zin=0.2/21.194u=9436.6 Ω

* Calculate Zout

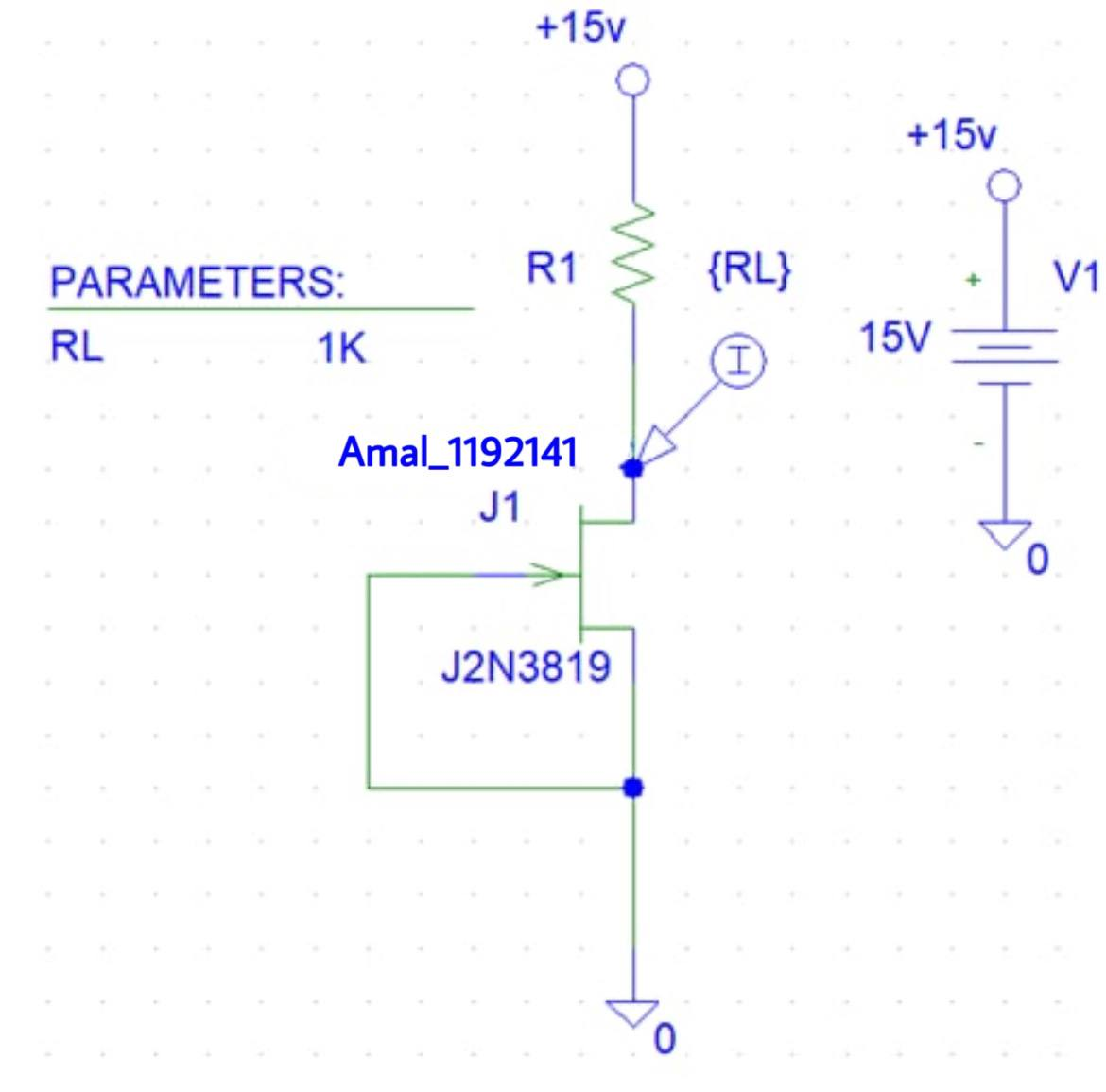


* Simulation of Iout



Zout=0.2/8.936u=22.38 KΩ

**Part C:** CONSTANT CURRENT SOURCE



Simulation of VL and ID



|  |  |  |
| --- | --- | --- |
| **RL(KΩ)** | **VL(V)** | **ID(mA)** |
| **0.1** | **1.23** | **12.003** |
| **0.22** | **2.634** | **11.96** |
| **0.33** | **3.95** | **11.93** |
| **0.47** | **5.58** | **11.889** |
| **0.56** | **6.62** | **11.862** |
| **1** | **11.7** | **11.73** |
| **1.5** | **13.44** | **8.9345** |
| **2** | **13.9** | **6.9508** |
| **3** | **14.3** | **4.768** |